REMARKS

Applicants respond hereby to the outstanding final Office Action dated February 14, 2008. Applicants amend claims 1, 3, 5, 6, 7, 8, 10, 11, 12 and 13 hereby, and cancel claims 2, 4, 9, 14 and 16, without prejudice or disclaimer of subject matter. Claims 1, 3, 5-8, 10-13, 15 and 17-20 are pending hereinafter, where claims 1 and 13 are the independent claims.

In the outstanding final Office Action, at paragraphs 3, the drawings were objected to under 37 CFR 1.83(a) as failing to show the limitations of claims 3 and 9, the Examiner requiring that the features be shown or the claims cancelled. At paragraphs 4 and 5 of the outstanding final Office Action, claims 1-20 were rejected under 35 USC §101, as merely disclosing a series of mental steps/components, and therefore asserted to be non-statutory. At paragraphs 6 and 7 of the outstanding final Office Action, the Examiner rejected claims 1-5 and 11-17 under 35 USC §102(b) as anticipated by US Patent No. 5,880,983 to Elliot, et al. (Elliot). At paragraphs 8 and 9 of the outstanding Office Action, the Examiner rejected claims 6-8 and 18-19 under 35 USC §103(a) as unpatentable over Elliot in view of US Patent No. 7,228,325, to Wilson, Jr., et al. (Wilson). Each of the drawing objections and rejections to the pending claims are made final by the outstanding final Office Action.

Drawing Objections

In response to the objections to the drawings under 37 CFR 1.83(a), applicants have cancelled claims 4, 9 and 16 without prejudice or disclaimer of subject matter, and amended claim 10 to depend from claim 8. Applicants also amend claim to remove reference to "means to compute," such that the aligner computes said shift amount based only on said exponent values. For that matter, based on the Examiner's comments, applicants also amend claim 6 to remove "means to

determine."

Claim 3 as amended now recites a floating point execution unit according to Claim 1, wherein the aligner computes a shift amount for aligning said product and the third operand and the multiplexer operates to select the third operand as the designer computes the shift amount. Claim 11 is dependent on claim 3, and claim 12 depends from claim 11. Claims 11 and 12 are amended to maintain consistency with the claim 3 language, as amended.

Claim 6 as amended now recites a floating point execution unit according to claim 1, wherein each of the operands has an exponent value, and floating point execution unit determines whether the exponent values of any of the operands is zero, in parallel with operation of the multiplier and the aligner. Claims 7 and 8, which depend from claim 6 are amended. The dependency of claim 10 is amended to depend from claim 8, instead of cancelled claim 9. Applicants respectfully assert that the drawings comply with 37 CFR 1.83(a), and request withdrawal of the drawing objections.

Rejections Under 35 USC §101

In response to the rejection of claims 1-20 under 35 USC §101, as directed to non-statutory subject matter, applicants respectfully assert that pending claims 1, 3, 5-8, 10-13, 15 and 17-20 comply fully with Section 101. At paragraph 5 of the outstanding final Office Action, the Examiner asserts that claims 1-20 recite a method and unit for performing multiplying/adding operation without further disclosing a practical/physical application, or useful and tangible result since the claims "preempt" every substantial practical application of the "idea" embodied by the claim, and that there is no cited limitation that breathes sufficient life and meaning into the preamble to limit to a particular application.

In response, applicants have substantially amended independent claims 1 and 13 to address the section 101 rejections as stated.

Independent claim 1 as amended sets a floating point execution unit for performing multiply/add operations on a floating point number comprising a plurality of operands taken from an instruction having a plurality of floating point number operand positions, the floating point unit comprising:

a multiplier for calculating a product of two of the operands;

an aligner coupled to the multiplier for aligning said product and a third of the operands;

a first data path for supplying to the multiplier operands from a first and a second of the operand positions of the instruction;

a second data path for supplying the third operand to the aligner; and

a multiplexer on the second data path for selecting, for use by the aligner, either the operand from the second operand position of the instruction or the operand from the third operand position of the instruction, and supplying same to the multiplier;

wherein the first data path is maintained free of multiplexer operations.

Independent claim 13 as amended sets forth method of operating a floating point execution unit to perform multiply/add operations on a floating point number, the floating point unit having a multiplier, an aligner coupled to the multiplier, and a multiplexer, the method comprising the steps:

sending an instruction to the floating point unit, the instruction having a plurality of operand positions holding operands of the floating point number;

using the multiplier to calculate a product of two of the operands of the instruction;

using the aligner to align said product and a third of the operands of the instruction;

supplying over a first data path to the multiplier operands from a first and a second of the operand positions of the instruction, wherein said first data path is free of multiplexer operations;

supplying over a second data path a third operand of the instruction to the aligner;

positioning the multiplexer on the second data path;

using the multiplexer to select, for use by the aligner, either the operand from the second operand position or the operand from the third operand position; and

outputting the selected operands to the aligner.

Both the claimed floating point execution unit and method of operating a floating point execution unit to perform multiply/add operations on floating point numbers, as amended, are directed to a machine and process, respectively, that operate on floating point numbers to generate a processed output. The claimed subject matter is not believed stand outside the scope of Section 101 because neither of independent claims 1 and 13 (as amended) merely comprise (recite) an abstract idea, law of nature or natural phenomenon. The amended floating point execution unit (claim 1) and method of operating a floating point execution unit (claim 13) are more than a series of mental steps/components for performing multiply/add operations.

The practical application resides in the fact that the unit and method both multiply/add floating point number operands, arriving in an instruction, and require no multiplexing in a first path to the multiplier for the first two operands of the instruction, and outputting a product and aligned floating point output. Applicants' floating point execution unit (claim 1) and method of operating a floating point execution unit (claim 13), increase the performance speed of a floating point execution unit (applicants' Specification at page 2, paragraph [0007]). Applicants' invention as claimed removes operand formatting/selection and unpacking from the timing critical path in floating point

execution, increasing performance of the floating point unit significantly (applicants' Specification at page 2, paragraph [0008]).

Applicants respectfully assert that independent claims 1 and 13 as amended, and claims 3, 5, 6, 7, 8, 10, 11 and 12 that depend from claim 1, and claims 15 and 17-20 that depend from claim 13, do not claim a mere principle, but a novel floating point unit, and a novel method of operating a floating point unit, which process a floating point number and output the processing result. As such, the claims provide a useful, tangible, concrete result (MPEP 2106) and are thought, and respectfully asserted to be statutory under 35 USC §101. Applicants, therefore, request withdrawal of the rejection of claims 1, 3, 5-8, 10-13, 15 and 17-20 thereunder.

Rejections Under 35 USC 102(b)

Claims 1-5 and 11-17 were rejected under 35 USC §102(b) as anticipated by Elliot. The Examiner asserts that Elliot at Fig. 2 discloses a floating point execution unit (Fig. 2) for performing multiply/add operations using a plurality of operands taken from an instruction with a plurality of operand positions **(A, B and C; col. 1, lines 21-50)**, the floating point execution unit comprising:

a multiplier **102** for calculating a product of two operands **(Elliott's operands A and C)**;

an aligner **118** coupled to the multiplier for combining the product and a third **(B)** of the operands;

a first data path for supplying to the multiplier operands from a first and second of the operand positions of the instruction **(Data feed path feeding A and C into multiplier 102)**;

a second data path for supplying to the third operand to the aligner **(data path feeding B into muxes 114, 116)**; and

a multiplexer **(114, 116)** on the second data path for selecting, for use by the aligner, either the operand from the second operand position of the instruction **(A)** or the operand from the third operand position of the instruction **(B)**.

The rejection is maintained as final in the outstanding final Office Action. In response, applicants have amended independent claims 1 and 13 to include the limitations of dependent claims 2 and 14, respectively. In view of the amendments to independent claims 1 and 13, and for at least the reasons set forth below, independent claims 1 and 13 are patentable over Elliott under 35 USC §102(b).

That is, while the Examiner asserts that Elliot discloses an aligner **118** coupled to the multiplier for combining the product **(A x C)** and a third **(B)** of the operands, applicants do not see the support in Elliot's Figs 2A and 2B. Multiplier (102) is not coupled Elliot's first aligner (118), but coupled to first and second multiplexers (114) and (116), respectively.

For that matter, while the Examiner asserts that Elliot discloses a first data path for supplying to the multiplier operands from a first and second of the operand positions of the instruction **(Data feed path feeding A and C into multiplier 102)**, applicants do not see the support for same in Elliot's Figs. 2A and 2B. Elliot' first path from multiplier (102) to first and second multiplexers (114) and (116) cannot be equivalent to applicants' claimed first data path because the Elliot first data path includes the two multiplexers. As amended, the independent claims now make clear that the first data path, and step of supplying over a first data path, are multiplexer free, where only the claimed second data path, and claimed step of supplying over a second data path perform any selecting.

While the Examiner asserts that Elliot discloses a second data path for supplying to the third operand to the aligner **(data path feeding B into muxes 114, 116),** this path is the same path as the first path, so cannot be equivalent to applicants' claimed second path. Applicants claimed first path uses no multiplexers, and their claimed second path does. Since Elliot's first path uses multiplexers 114 and 116, and operand B uses multiplexers 114 and 116, either Elliot's first path is different than applicants' claimed first path, or Elliot does not include a second path as claimed.

Applicants, therefore, respectfully assert that Elliot does not include each of the elements of applicants' independent claims 1 and 13, and independent claims 1 and 13 are patentable under Section 102(b) in view of Elliott. Claims 3, 5 and 11-12 depend from claim 1 and are patentable therewith, and claims 15 and 17 depend from claim 13 and are patentable therewith. Hence, applicants respectfully request withdrawal of the rejection of claims 1, 3, 5 and 11-13, 15 and 17 under section 102(b) in view of Elliott.

Rejections Under 35 USC §103(a)

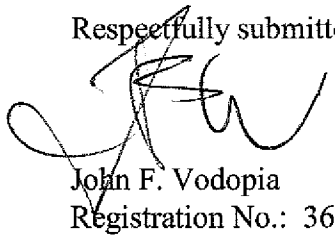
Claims 6-8 and 18-19 were rejected under 36 USC §103(a) as unpatentable over Elliott in view of Willson. The Examiner asserts that Elliott fails to disclose that each of the operands has an exponent value, and further comprises means, operating in parallel with the multiplier and the aligner, to determine whether the exponent values of any of the operands is 0 while the multiplier calculates the product to establish a test result number," but that Willson does, and that it would have been obvious in order to conserve power to combine Willson's feature at col. 7, line 60-col. 8, line 15, with Elliott to realize the invention as set forth in claims 6-8 and 18-19. Applicants respectfully disagree.

As mentioned above in response to the rejection of independent claims 1 and 13 under Section 102(b) in view of Elliott, Elliot does not teach each of the limitations, or the equivalents, of applicants' independent claims 1 and 13 (as amended). Because Elliott does not anticipate claims 1 and 13 under the law, Elliot does not include each of the limitations of amended independent claims 1 and 13. Hence, combining Elliott with Willson, even assuming arguendo that Willson includes the limitations as asserted in the final Office Action cannot realize applicants' invention as set forth in claims 6-8 and 18-19, for at least the reasons set forth above for the patentability of amended independent claims 1 and 13 in view of Elliott under Section 102(b). Applicants respectfully request, therefore, that the rejection of claims 6-8 and 18-19 under section 103(a) over Elliott in view of Willson be withdrawn.

Conclusion

It follows that each of pending claims 1, 3, 5-8 and 10-13, 15-20 is statutory under section 101, and is patentably distinct from Elliott, whether under Section 102(b) or combined with Willson under Section 103(a). If the Examiner believes that a telephone conference with applicant's attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully submitted,



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